Application number 09/881,226   <u>PATENT</u>
Amendment dated April, 9, 2004
Reply to office action mailed March 9, 2004

<u>Amendments to the Claims:</u>

This listing of claims will replace all prior versions, and listings of claims in the application:

<u>Listing of Claims:</u>

Claim 1 (original)   A programmable logic integrated circuit comprising:

a programmable logic portion; and

an embedded processor portion coupled to the programmable logic portion and comprising:

a processor; and

a memory block coupled to the processor and comprising:

a memory having a first port and a second port; and

an arbiter coupled to the first port and the second port, wherein the arbiter arbitrates access to the memory by the first port and the second port.

Claim 2 (original)   The integrated circuit of claim 1 wherein the memory is a dual-port SRAM.

Claim 3 (original)   The integrated circuit of claim 2 wherein the programmable logic portion comprises a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered logic functions.

Claim 4 (original)   The integrated circuit of claim 3 wherein the programmable logic portion further comprises a plurality of horizontal and vertical interconnect lines, programmably coupled to the plurality of logic elements.

Claim 5 (original)   The integrated circuit of claim 1 wherein the second port is configurable in width and depth.

Claim 6 (original)   The integrated circuit of claim 1 wherein the first port and the second port are both configurable in width and depth.

Claim 7 (original)   A programmable logic integrated circuit comprising:

a programmable logic portion comprising a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered logic functions; and

an embedded processor portion coupled to the programmable logic portion and comprising:

a processor; and

a memory block coupled to the processor and comprising:

a first plurality of memory cells for storing data;

a second plurality of memory cells for storing data;

a first port coupled to the first and second pluralities of memory cells;

a second port coupled to the first and second pluralities of memory cells; and

an arbiter coupled to the first port and the second port,

wherein when the second port is accessing the first plurality of memory cells, the arbiter prevents the first port from accessing the first plurality of memory cells, and when the second port is accessing the first plurality of memory cells, the arbiter allows the first port to access the second plurality of memory cells.

Claim 8 (original)   The integrated circuit of claim 7 wherein the first plurality of memory cells and the second plurality of memory cells are defined by a user-programmable lock register.

Claim 9 (original)   The integrated circuit of claim 8 wherein the first and second pluralities of memory cells comprise a portion of a dual-port SRAM.

Claim 10 (original)   The integrated circuit of claim 9 wherein the programmable logic portion further comprises a plurality of horizontal and vertical interconnect lines, programmably coupled to the plurality of logic elements.

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          Claim 11 (original)   The integrated circuit of claim 10 wherein the second port is configurable in width and depth.

          Claim 12 (original)   The integrated circuit of claim 10 wherein the first port and the second port are both configurable in width and depth.

Claims 13-45 (cancelled)